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Low Power Three Stage Operational Transconductance Amplifier Design

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Abstract: An operational transconductance-amplifier (OTA) is basically designed for low voltage and low power applications. Bulk driven technique is widely used for the low supply voltage applications in the analog circuits, but it has another drawbacks such as low gain , low slew rate , and low bandwidth. In this paper, cascade technique is used the overcome the problem of the low gain, slew rate and low bandwidth. The proposed bulk driven three stage OTA is implemented with the use of cascoding technique. The 65nm CMOS technology is used for the designing of the proposed three stage OTA circuit. The measured results of the simulation shows that the proposed three stage OTA circuit requires the power consumption of 124.3µW and slew rate of 77.20 V/us. It also improves the gain, bandwidth of the bulk driven OTA.

Keyword: Moore's Law, CMOS technology, Cascoding technique, OTA.

I. INTRODUCTION

The operational tranconductance amplifier is the favorable active building block of analog circuits and system [1]. The Operational tranconductance amplifier is a popular analog circuit, basically used as the voltage to current converter device. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback [2]. It is difficult to design the analog circuit comparison with the digital circuit. The main issue that comes is the power consumption and voltage requirement while designing the analog circuit. In the modern era, Low power consumption is the main requirement of the portable and battery operated system. Reducing power consumption in portable applications has made lower supply voltages increasingly common in systems with large digital content [3].

Fast, High- Gain, Operational Transconductance Ampler (OTAs) are an integral part of switched-capacitor (SC) circuits [4]. The symbol the OTA is similar to the operational amplifier as shown in fig. 1. It has two input terminal one is inverting V_{in-} and other is non-inverting terminal V_{in+}, finally it has one output terminal that has current at the output I_{out}. OTA works as voltage controlled current source, its takes the difference of the two voltages as the input for the current conversion**.** OTAs are versatile analog building blocks that allow the amplification and filtering of signals with minimum power consumption [5]. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage. The negative feedback provides the gain control mechanism, it stabilizes the gain. Fig. 2 shows the equivalent circuit of the operational transoconductance amplifier, where output current depends on voltage of the inverting and non-inverting terminal.

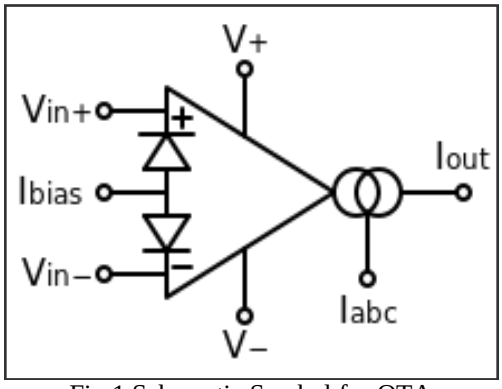

Fig.1 Schematic Symbol for OTA

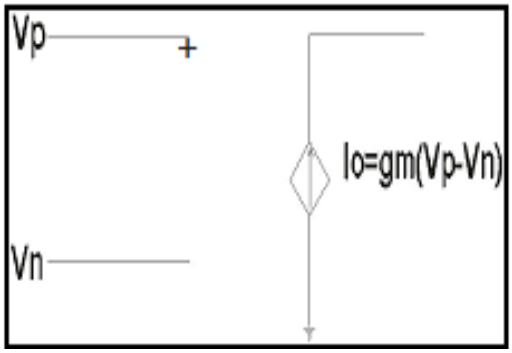

Fig. 2 Equivalent Circuit

I_{abc} input bias current is used to control the transconductance of the amplifier. I_{abc} is called bias current of the amplifier. Amplifier gain can be controlled with the help of bias current. I_{abc} is directly proportional to the amplifier's transconductance. Later version of the OTA uses another input current I_{bias} to control the diodes connected at the input. Cathode of the first diode is

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connected to the non inverting terminal (V_{in}+) and cathode of the second diode is connected to the inverting terminal (V_{in}-). Biasing of the diode is done with the help of applying current (I_{bias}) to the anodes terminal. The operational transconductance amplifier (OTA) works as the voltage to current converter device. In the ideal condition OTA, the output current of the OTA follows the differential input voltage. The expression of the output current of the OTA is as follows

$$I_{out} = (V_{in+} - V_{in-})g_m \qquad (1)$$

Where V_{in+} is the voltage at the non-inverting input, V_{in-} is the voltage at the inverting input. When input is applied to the inverting terminal of the OTA, output is out of phase of the input signal. G_m is the transconductance of the amplifier. I_{out} is the output current of the OTA, g_m is transconductance gain is given by:-

$$\sqrt{2kI_B} \qquad (2)$$

Where trasconductance parameter $k = \mu C_{ox} W/2L$, μ is the mobility of the carrier, C_{ox} is the capacitor per unit area. W is the width and L is the effective channel length.

A. Application of OTA

The OTA is used for implementation of voltage controlled oscillators (VCO) and filters (VCF) for analog music synthesizers. Another application of OTA includes in the implementation of an electrically tunable resistor that can be used as reference to ground. The primary application for an OTA is to drive low-impedance sinks such as coaxial cable with low distortion at high bandwidth. It is used in designing of active filters, portable devices, sensor implementation, and hearing aid implementation. OTAs (operational transconductance amplifiers) are versatile building blocks used for many applications such as filters, oscillators etc [6]**.** Examples of low-power applications that can benefit from the reduced supply voltage include portable products, biomedical and sensor implementations, hearing-aid devices, and energy harvesting applications [5]. OTA is also used in designing of Active filter. Transconductance – capacitor (G_m-C) filter have been used at hearing aids, pacemakers other low applications. Some Applications of the OTA is given as follows-

- **Voltage Amplifiers**

The basic voltage amplifier can be realized with the help of OTA circuit as shown in fig.3. The input signal is applied at the inverting terminal of the amplifier with the negative feedback. The negative feedback is used to provide the controllable gain to the amplifier. The expression of the voltage gain and output impedance is given as in equation 2 and 3.

$$\frac{V_0}{V_i} = \frac{1-g_m R_2}{1+g_m R_1} \qquad (3)$$

$$Z_o = \frac{R_1+R_2}{1+g_m R_1} \qquad (4)$$

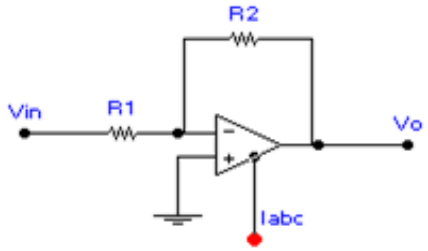

Fig. 3 Basic voltage amplifier circuit

Equation 3 and 4 reduces to equation 5 and 6 for the case $g_m R_1 >> 1$as given below

$$\frac{V_0}{V_i} = \frac{-R2}{R1} \qquad (5)$$

$$Z_o = \frac{R_1+R_2}{g_m R_1} \qquad (6)$$

Equation 3 is same as the voltage gain of a non-inverting amplifier. Finally OTA is working as the voltage amplifier.

- **Active Filters with the OTA**

Another application of the OTA is as a active filter It can be used to realize different type of filter, such as low pass filter, high pass filter notch filter etc. > Active filters can be realized with the help of OpAmps but OTA-based active filters can use the external bias setting to control the location of the critical frequency, or 3-dB frequency in a filter. A number of other active filters can be realized with the OTA. Some OTA based active filter is used to provide the ability to change the critical frequency, the gain, also with the preserving the shape of the response. OTA based active filters provides the facilty to control the critical frequency of the filter, without changing the passband ripple facility to change the type of response of the filter from low pass to allpass to highpass by adjusting the transconductance g_m. A simple example of a first-order lowpass filter is shown in Fig. 4. The voltage gain and 3-dB frequency is given as

$$\frac{V_o}{V_i} = \frac{g_m}{sC+g_m} \qquad (7)$$

$$f_{3dB} = \frac{g_m}{2\pi C} \qquad (8)$$

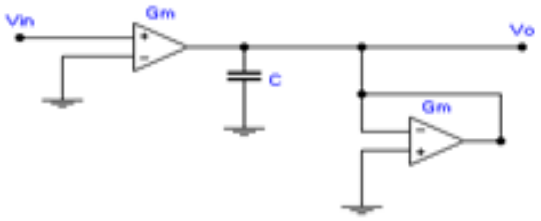

Fig. 4 Low Pass filter with OTA

In this circuit the second OTA, labeled "Gm2", is configured as a voltage variable resistor. It is this variable resistor which provides the variable cut-off frequency.

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B. Power Consumption

Power Consumption is the important parameter for the any type of the circuit. Power consumption is the basic constraints of any type of integrated circuit(IC). There is a trade-off between power and performance of any kind of integrated circuit(IC). The market for portable applications is a constantly evolving industry, and as a result, there is a huge demand for low-voltage low-power operation circuits [7]. Depending upon the application of the device or upon the purpose of the application to be performed, the inputs to the circuit device may vary from two to three [8]. Today leakage power has become an increasingly important issue in processor hardware and software design [9]. With the main component of leakage, the sub-threshold current, exponentially increasing with decreasing device dimensions, leakage commands an ever increasing share in the processor power consumption [10]. Leakage current is a primary concern for low-power, high-performance digital CMOS circuits [11]. The cost of the system is directly related to the power. In power dissipation, power is converted to heat and then radiated away from the device. If an IC is consuming more power, then a better cooling mechanism would be required to keep the circuit in normal conditions. Due to this generated heat, device may get damaged on continuous use. Power dissipation in CMOS circuits is the combination of three main components.

- Static (leakage) power dissipation
- Short circuit power dissipation
- Dynamic (switching) power dissipation

• Static Power Dissipation

Static power dissipation is related to logical states of the circuits and it is independent of switching activities. The static power dissipation of a circuit is defined as the product of the device leakage current and the supply voltage. Total static power dissipation is-

$$P_{stat} = I_{stat} V_{DD} \qquad (9)$$

Where I_{sat} is the current that flows through the circuit when there is no switching event and V_{DD} is the supply voltage.

• Short Circuit Power Dissipation

Short-circuit power dissipation in CMOS inverter occurs for finite rise and fall times of input voltage waveforms. A direct current path is formed, When both NMOS and PMOS transistors are turned on in the circuit simultaneously for a short duration of time during switching, This causes a direct current path between powers supply and ground.

• Dynamic Power Dissipation

Dynamic power dissipation is due to the power dissipation during switching activity. When frequency increases the switching activity is increases. This leads to the increase in power dissipation due to increase in switch activity. The most of the power dissipation in CMOS circuits is due to the charging/discharging of load capacitance.

C. Slew Rate

The slew Rate of an amplifier circuit is defined as the maximum rate of change of the output voltage per unit time. Slew Rate is usually expressed in units of V/µs.

$$\text{Slew Rate} = \max.\left(\frac{dVout\ (t)}{dt}\right) \qquad (10)$$

D. CMRR (Common Mode Rejection Ratio)

The Common - Mode Rejection Ratio (CMRR) of a differential amplifier defines the ability of the device to reject common-mode signals. Common-mode signals appear simultaneously and in-phase on both inputs of the amplifiers. An ideal differential amplifier would have infinite CMRR but this is not practically possible. A high CMRR is required to amplify differential signal in the presence of a possibly large common-mode input. The CMRR of the OTA should be as high as possible.

$$CMRR = A_d/A_c = 20\log_{10}(A_d/A_c)\ dB \qquad (11)$$

II. TECHNOLOGY SCALING

With the advancement of very large scale integrated circuit technology, there is a huge demand of the more efficient integrated circuit in the electronic market now days. Over the past several years, silicon CMOS technology has become the dominant fabrication process for relatively high performance & cost effective VLSI circuit [12]. So the requirement of the low power IC's is increasing with the increasing demand of battery operated electronics products and portable devices in the electronic market. The battery operated devices must be designed to work on less power consumption because batteries provide limited power supply to the devices. Technological scaling- down sustains System-on-Chip (SoC) trend. Scaling of the CMOS technology improves the performance of the integrated circuit, increases the transistor density and reduces the power consumption. The scaling down of feature size generally leads to improve performance and it is important therefore to understand thev effect of scaling. [12]. There are basically three main goals of the scaling CMOS technology from present generation to next generation.

- It reduces the gate delay by 30%. This result in the increase in the operating frequency of about 43%.
- It increases the transistor density twice. This result in the area reduction of the integrated circuit.
- It reduces energy per transistor approximately 65% that results in power saving of 50% for increased frequency range.

The demand of these devices depends on various factor such that higher speed, lower delay, low area, low power consumption, small silicon area, longer battery life and high reliability [6]. Also large power dissipation requires

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expensive and noise cooling machinery, batteries and power conservation circuits [7].
. The reduction of power consumption is a crucial task for battery-operated applications, such as energy-harvested-operated microsensor nodes, biomedical implantable devices and microsystems in general [13,14].

III. BULK DRIVEN TECHNOLOGY

One of the most common techniques is bulk driven technology to achieve rail to rail input operating range. Bulk driven technique is used for the low power application. Bulk driven transistor is same as to the gate driven transistor but only difference that ac input signal in applied to the bulk terminal for the creation of conduction between source and drain terminal shown in Fig. 5. Threshold voltage requirement in the bulk driven transistor is lower that the gate driven transistor.

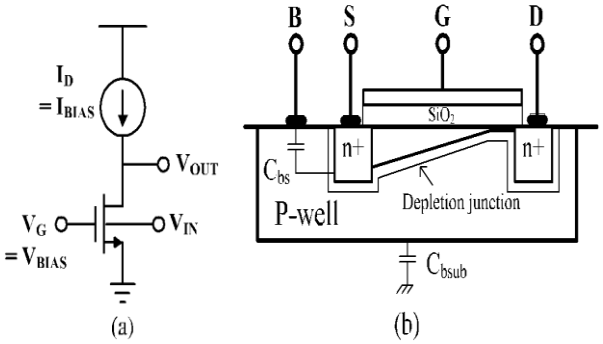

Fig.5 Bulk-driven NMOS transistor: (a) circuit operation; (b) cross section [5]

The limit of the minimum threshold voltage is increased with the Bulk driven technology that is the advancement in the gate driven technology where voltage supply requirement is limited by the threshold voltage. The result of this concept is that bulk-driven transistor operates on the same principle as junction-field-effect-transistor (JFET) is operated in its depletion mode. For illustration purposes, a cross section of the bulk-driven transistor is shown in Fig. 5(b) [5].

IV. CASCODE TECHNIQUE

There are three ways in which the gain could be increased
1. Add additional gain stages.
2. Increase the tranconductance of the first or second stage
3. Increase the output resistance seen by the first or second stage [15].

Third technique is more attractive because the output resistance increases in proportion to a decrease in bias current. The cascode is a two-stage amplifier comprising a common emitter stage feeding into a common base stage [16, 17].
Multistage amplifier provides high input impedance, high output, higher gain, high bandwidth, higher input-output isolation compared to a single amplifier stage. In modern circuits, casocde can be constructed from Bipolar junction transistor or Metal Field effect transistor, with one terminal operating as a common emitter or common source and the other as a common base or common gate. The cascode improves input-output isolation (or reverse transmission) as there is no direct coupling from the output to input. The cascade technique is used to eliminate the Miller effect and provides higher bandwidth.

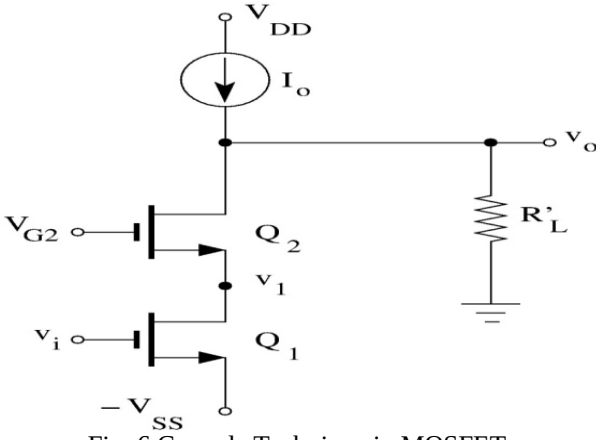

Fig. 6 Cascode Technique in MOSFET

Fig. 6 shows an example of a cascode amplifier with a common source amplifier as the input stage driven by an input signal source V_{in}. The input stage of the common source is used to drive a common gate amplifier as the output stage, with output signal V_{out}. The lower MOSFET is conducted by providing a gate voltage but the upper MOSFET conducts with the help of potential difference across its gate and source. The major advantage of this circuit arrangement stems from the placement of the upper field-effect transistor (FET) as the load of the input (lower) FET's output terminal (drain). The upper MOSFET gate is effectively grounded at operating frequency but the upper MOSFET source voltage is kept during operation. In other words we can say the upper MOSFET provides a low input resistance to the lower MOSFET and is used to provide low voltage gain to the lower MOSFET, which provides a large amount of reduction in the the Miller feedback capacitance from the lower MOSFET's drain to gate. The loss of the voltage gain is recovered with the help of upper MOSFET. Thus, the upper transistor allows the lower FET to operate with minimum negative (Miller) feedback that causes the improvement in its bandwidth. The upper MOSFET gate terminal is electrically grounded, so charge and discharge of the stray capacitance, C_{dg}, between drain and gate is simply through R_D and the output load (say R_{out}). Thus the frequency response is affected only for frequencies above the associated RC time constant: If the upper MOSFET stage were operated alone using its source as input node that is common gate (CG) configuration, it would have a good voltage gain and wide bandwidth. However, its low input impedance would limit its usefulness to very-low impedance voltage drivers. Addition of the lower

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MOSFET is used to provide high input impedance that allows the cascode stage to be driven by a high impedance source. If the upper MOSFET is replace by the inductance or resistive load and output is taken from the MOSFET drain that is common source configuration.

The Common Source configuration would provide same input impedance as the cascade configuration would provide greater gain and bandwidth.

- **Stability**

The cascade arrangement provides better stability. Its output is electrically and physically isolated from the input both. The lower transistor has nearly constant voltage at both drain and source and thus there is essentially "nothing" to feed back into its gate. The upper transistor has nearly constant voltage at its gate and source. Thus practically there is a small amount of feedback from the output to the input. Metal shielding is both effective and easy to provide between the two transistors for even greater isolation when required. This would be difficult in one-transistor amplifier circuits, which at high frequencies would require neutralization.

- **Biasing**

As shown in fig. 6, the cascode circuit uses two "stacked" MOSFETs provides some restrictions on the two MOSFETs namely, the upper FET must be biased so its source voltage is kept high but the lower FET drain voltage may swing too low, causing it to saturate. MOSFETs require careful selection for the pair because special biasing of the upper MOSFET gate increases cost. The cascode circuit can also be built with the help of bipolar transistors, or MOSFETs, or one FET (or MOSFET) and one BJT can also be used for the designing. This circuit arrangement was very common in VHF television tuners when they employed Vacuum tubes.

- **Advantages**

The cascode arrangement offers high gain, high bandwidth, high slew rate, high stability, and high input impedance.

- **Disadvantages**

The cascode circuit requires two transistors and requires a relatively high supply voltage. For the two-FET cascode, both transistors must be biased with ample V_{DS} in operation, imposing a lower limit on the supply voltage.

- **Application of Cascode**

With the rise of integrated circuits, transistors have become cheap in terms of silicon die area. In MOSFET technology especially, cascoding can be used in current mirrors to increase the output impedance of the output current source. A modified version of the cascode can also be used as a modulator, particularly for amplitude modulation. The upper device supplies the audio signal, and the lower is the RF amplifier device.

V. PROPOSED THREE STAGE OTA

The proposed design of the three stage operational transconductance amplifier is shown in fig. 7 using 65nm CMOS technology. Proposed circuit of the three stage operational transconductance amplifier uses the cascading technique at the common source amplifier stage. The caoscode technique is nother but stacking of the transisitors. The common source stage is basically second stage in the three stage OTA circuit. This causes the increase in the gain, slew rate, bandwidth, stability, and input impedance. The design is added with two transistors M9 and M10 that are used as cascaded transistor used with M3 and M5. Result of adding two transistors improve gain, stability, bandwidth and reduce power consumption. Table 1 shows the transistor dimensions of the proposed circuit of the operational transconductance amplifier. Fig. 8 shows the transient response of the proposed three stage Operational Transconductance Amplifier circuit.

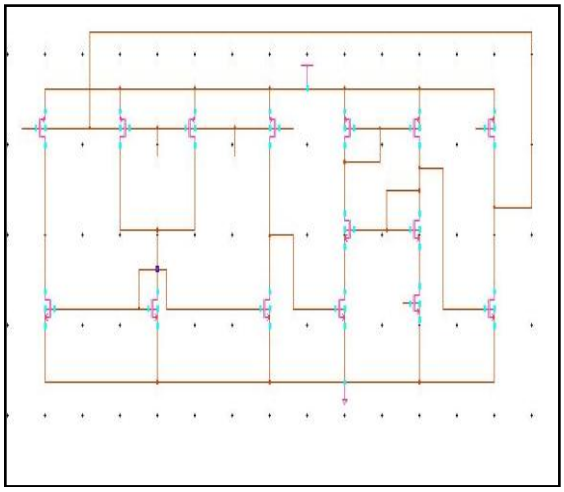

Fig.7 Proposed Three stage OTA circuit

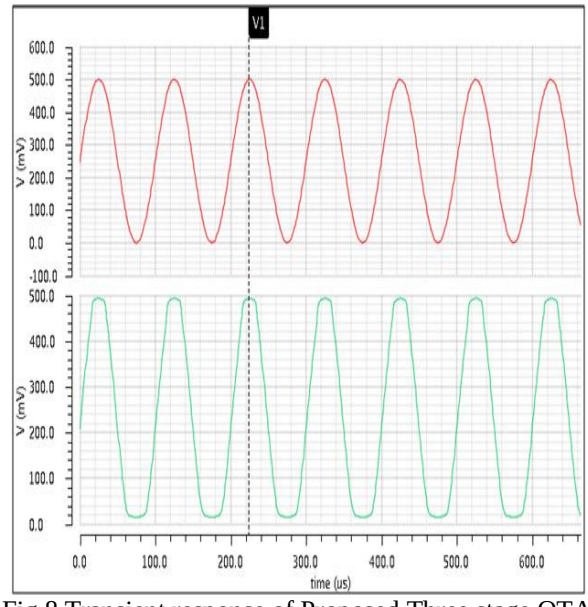

Fig 8 Transient response of Proposed Three stage OTA circuit

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Waveform shows that proposed circuit is behaving as the voltage follower by applying the unity feedback gain. The gain waveform of the operational transconductance amplifier in fig. 9 shows the gain is approximately 45.63 dB. Simulated results at supply voltage Vdd=0.5V shows power consumption and slew rate is approximately 124.029 µW and 77.2024 V/µs. The simulated value of the power consumption and slew rate is shown in fig. 10 and fig.11.

TABLE 1

Transistor	Weight	Length
M1	65µm	160nm
M2	64µm	160nm
M3	52µm	160nm
M4	128µm	160nm
M5	52µm	60nm
M6	128µm	60nm
M7	65µm	60nm
M8	65 µm	60nm
$M9_{new}$	128 µm	60nm
$M10_{new}$	128 µm	60nm

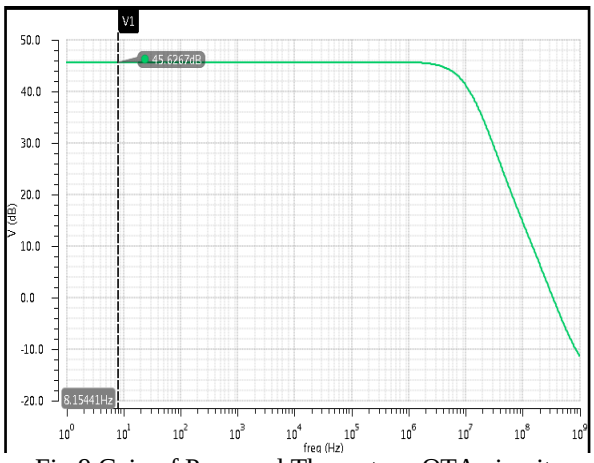

Fig 9 Gain of Proposed Three stage OTA circuit

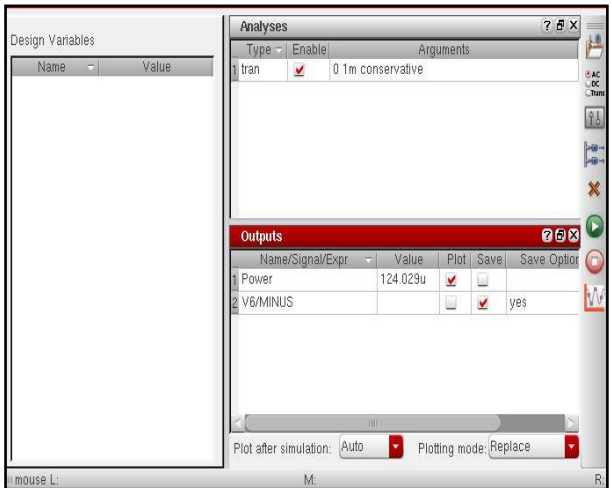

Fig .10 Power Consumption of proposed three stage OTA circuit

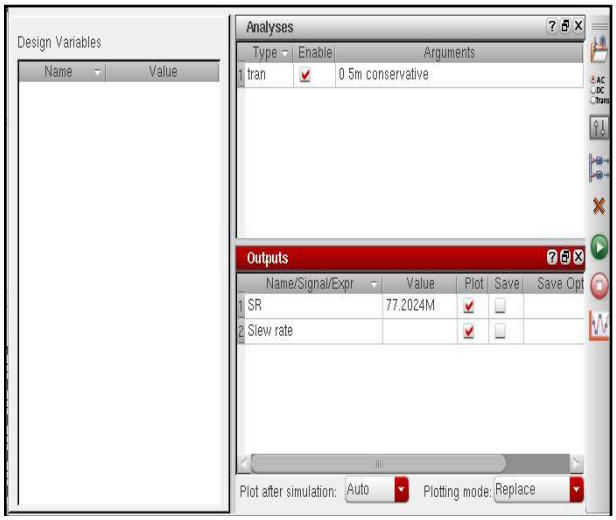

Fig. 11 Slew Rate of proposed three stage OTA circuit

Table 2.shows the parameter of the proposed three stage operational tranconductance amplifier circuit. From the table it is clear that the proposed three stage operational transconductance amplifier circuit with the cascading technique has reduced the power consumption, improve the gain, unity gain frequency and slew rate.

TABLE 2

Parameters	Proposed three Stage OTA
Supply Voltage(V)	0.5
Power (µW)	124.03
Gain (dB)	45.63 dB
Unity Gain Frequency (MHz)	309.03
Slew Rate(V/us)	77.20

VI. CONCLUSION

Simulation of the design is done on the 65nm CMOS technology. This work reveals that operational transconductance amplifier circuit using cascading technique to reduce the power consumption. Multi stage OTA has better performance comparing the two stage OTA. In this paper, three Stage Operational transoconductance amplifier has designed with the bulk drive technology that allows it to operate at low voltage. The Proposed circuit uses the cascoding technique to stack the transistors in the second stage of the three stage OTA. This reduces the power consumption of the three stage OTA, increases gain and bandwidth, also improves the slew rate. The proposed OTA circuit requires the power consumption of 124.3µW and slew rate of 77.20 V/us.

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